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EXAMINER	
RODRIGUEZ, GLENDA P	
ART UNIT	**PAPER NUMBER**
2651	

DATE MAILED: 02/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/993,779	OZDEMIR, HAKAN	
	Examiner	Art Unit	
	Glenda P. Rodriguez	2651	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/30/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> > (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Reed et al. (US Patent No. 6, 144, 513).

Regarding Claim 1, Reed et al. teach a head-connection-polarity detector, comprising:

A circuit operable to recover servo data from a servo signal generated by a read-write head that is coupled to the circuit with a connection polarity (Col. 4, Lines 54-67. Reed et al. teach a circuit that receives inputted data from the head and detects the polarity of the servo signal from that data.);

And a determinator coupled to the circuit and operable to determine the connection polarity from the recovered servo data (Col. 4, Lines 54-67 and Col. 11, Lines 54-67. Reed et al. teach of a circuit that determines if the polarity pulses are positive or negative. And Col. 13, L. 11-58, wherein the phase is corrected in order for the head to make the head be connected as shown in the Applicant's Specification in paragraph [27].).

Regarding Claim 2, Reed et al. teach all the limitations of Claim 1. Reed et al. further teach the circuit is operable to recover a servo-synchronization mark from the servo signal (Col. 4,

Lines 54-67 and Col.. 7, Lines 33-38and Col. 9, Lines 50-59. Reed et al. teach a circuit that receives inputted data from the head and detects the polarity of the servo signal from that data.); and the determinator is operable to determine the connection polarity from the recovered servo-synchronization mark (Col. 4, Lines 54-67 and Col. 11, Lines 54-67. Reed et al. teach of a circuit that determines if the polarity pulses are positive or negative.).

Regarding Claim 3, Reed et al. teach all the limitations of Claim 1. Reed et al. further teach wherein the deteminator is operable to generate a signal that indicates the determined connection polarity (Col. 11, Lines 54-67. Reed et al. teach a $SBIT_n$ signal being high when a positive polarity signal is detected and $SBIT_n$ being low when it is a negative pulse.).

Regarding Claim 4, Reed et al. teach all the limitations of Claim 1. Reed et al. further teach wherein the circuit comprises a Viterbi detector (Col. 4, Line 67 to Col. 5, Line 3).

Regarding Claim 5, Reed et al. teach all the limitations of Claim 1. Reed et al. teach wherein the circuit is operable to recover the servo data from the servo signal regardless of the connection polarity (Col. 12, Lines 6-13).

Regarding Claim 49, Reed et al. teach a method, comprising:

Sampling a servo signal having a phase (See Abstract and Col. 11, Lines 39-61);

And recovering servo data from the servo signal regardless of the phase of the servo signal (Col. 11, Lines 39-61 and Col. 13, L. 11-58).

2. Claim 6-22, 23, 27, 28-33, 36-41 24, 34 and 35 are rejected under 35 U.S.C. 102(e) as being anticipated by Tuttle et al. (US Patent No. 6, 108, 151).

Regarding Claim 21, Tuttle et al. teach a synchronization-and-head-connection polarity detector, comprising:

A Viterbi detector operable to recover a synchronization mark from samples of the servo signal generated by a read head that is coupled to the Viterbi detector with a connection polarity (Col. 20, Lines 15-22. Tuttle et al. teach that the Viterbi detector could also be used for synchronously detecting data. See also Col. 12, L.5-60 wherein the phase is corrected in order for the head to make the head be connected as shown in the Applicant's Specification in paragraph [27].);

A comparator coupled to the Viterbi detector and operable to determine the connection polarity from the recovered synchronization mark (Col. 19, Line 65 to Col. 20, Line 11. Tuttle et al. teaches that the device detects if the pulse is positive or negative. See also Col. 12, L.5-60.).

Regarding Claim 22, Tuttle et al. teach all the limitations of Claim 21. Tuttle et al. further teach wherein the comparator is operable to generate a signal that indicates the determined connection polarity (Col. 19, Line 65 to Col. 20, Line 11. Reed et al. teach a $SBIT_n$ signal being high when a positive polarity signal is detected and $SBIT_n$ being low when it is a negative pulse.).

Regarding Claim 23, Tuttle et al. teach all the limitations of Claim 21. Tuttle further teach wherein the Viterbi detector is operable to recover the synchronization mark from the servo signal regardless of the connection polarity of the read head (Col. 20, Lines 17-22).

Regarding Claim 27 and 33, Tuttle et al. teach a servo channel, comprising:

A sampling circuit coupled to receive and operable to generate samples of a servo signal that represents a servo-synchronization mark and that has a phase (Col. 8, Lines 48-51 and Lines 56-59);

And a synchronization-mark-and-polarity detector coupled to the sampling circuit and comprising,

A first Viterbi detector operable to recover the synchronization mark from the samples of the servo signal (Col. 20, Lines 15-22. Tuttle et al. teach that the Viterbi detector could also be used for synchronously detecting data.);

And a comparator coupled to the first Viterbi detector and operable to determine the phase of the servo signal from the recovered synchronization mark (Col. 19, Line 65 to Col. 20, Line 11. Tuttle et al. teaches that the device detects if the pulse is positive or negative. See also Col. 12, L.5-60 wherein the phase is corrected in order for the head to make the head be connected as shown in the Applicant's Specification in paragraph [27].).

Regarding Claim 28, Tuttle et al. teach all the limitations of Claim 27. Tuttle et al. further teach the comparator is coupled to the sampling circuit and the sampling circuit is operable to generate the samples of the servo signal having a desired phase (Col. 8, Lines 48-51 and Lines 56-59 and Col. 19, Line 65 to Col. 20, Line 11. Tuttle et al. teaches that the device detects if the pulse is positive or negative.).

Regarding Claim 29, Tuttle et al. teach all the limitations of Claim 27. Tuttle et al. further teach the comparator is coupled to the sampling circuit (Col. 19, Line 65 to Col. 20, Line 11 and Col. 8, Lines 48-51 and Lines 56-59. Tuttle et al. teaches that the device detects if the pulse is positive or negative.); and the sampling circuit is operable to generate the samples of the servo signal having a desired phase (Col. 11, Lines 30-38. Tuttle et al. teaches a phase circuit that

determines the phase of the current signal, calculates a phase error and then adjusting the phase of the signal to the desired phase.).

Regarding Claim 30, Tuttle et al. teaches all the limitations of Claim 27. Tuttle et al. further teach the comparator is operable to generate a phase signal that indicates the determined phase; and the sampling circuit is coupled to the phase determinator and is operable to generate the samples of the servo signal having a desired phase in response to the phase signal (Col. 8, Lines 48-51 and Lines 56-59 and Col. 11, Lines 30-48 and 46-50).

Regarding Claim 31, Tuttle et al. teach all the limitations of Claim 27. Tuttle et al. further teach wherein the phase of the servo signal represents a connection polarity between the sampling circuit and a read head that generates the servo signal (Col. 14, Lines 16-24).

Regarding Claim 32, Tuttle et al. teach all the limitations of Claim 27. Tuttle et al. further teach comprising: wherein the servo signal also represents servo data other than the synchronization mark (Col. 6, Lines 34-37. Tuttle et al. teaches that detects user data.); and a second Viterbi detector coupled to the sampling circuit and operable to recover the other servo data from the samples of the servo signal (Col. 20, Lines 17-22 and Col. 8, Lines 48-51 and Lines 56-59 and Col. 11, Lines 30-48 and 46-50. Tuttle et al. teaches that the device detects if the pulse is positive or negative.).

Regarding Claim 36, Tuttle et al. teach a disk-drive system, comprising:

A data-storage disk having a surface and operable to store a servo synchronization mark and other servo data (Col. 4, Lines 28-47);

A motor coupled to and operable to rotate the disk (It is inherent in the art that the disk is driven by a motor (also called spindle motor).);

A read head operable to generate a servo signal that has a phase and that represents the synchronization mark and the other servo data;

A read-head positioning assembly operable to move the read head over the surface of the disk (Col. 4, Lines 13-20);

And a servo channel coupled to the read head, the servo channel comprising,

A sampling circuit operable to generate samples of the servo signal and to adjust a phase of the samples to a desired value in response to a determined phase of the servo signal (Col. 8, Lines 48-51 and Lines 56-59. Tuttle et al. further teach that the read data is binary data. See also Col. 12, L.5-60 wherein the phase is corrected in order for the head to make the head be connected as shown in the Applicant's Specification in paragraph [27].),

A synchronization-mark-and-coupling- -polarity detector coupled to the sampling circuit and comprising,

A first Viterbi detector operable to recover the synchronization mark from the samples of the servo signal, and a comparator coupled to the first Viterbi detector and operable to determine the phase of the servo signal from the recovered synchronization mark and to provide the determined phase to the sampling circuit (Fig. 7 and Col. 11, Lines 30-50. See also Col. 12, L.5-60 wherein the phase is corrected in order for the head to make the head be connected as shown in the Applicant's Specification in paragraph [27].),

And a second Viterbi detector coupled to the sampling circuit and operable to recover the other servo data from the samples of the servo signal (Col. 8, Line 67 to Col. 9, Line 2).

Regarding Claim 37, Tuttle et al. teach a disk-drive system, comprising:

A data-storage disk having a surface and operable to store a servo synchronization mark and other servo data (Col. 4, Lines 28-47);

A motor coupled to and operable to rotate the disk (It is inherent in the art that the disk is driven by a motor (also called spindle motor).);

A read head operable to generate a servo signal that has a phase and that represents the synchronization mark and the other servo data (Col. 15, Lines 13-30);

A read-head positioning assembly operable to move the read head over the surface of the disk (Col. 4, Lines 13-20);

And a servo channel coupled to the read head, the servo channel comprising,

A sampling circuit operable to generate samples of the servo signal (Col. 8, Lines 48-51 and Lines 56-59. Tuttle et al. further teach that the read data is binary data.),

And a Viterbi detector operable to recover the synchronization mark and other servo data from the samples of the servo signal regardless of the phase of the servo signal (Col. 20, Lines 17-22. See also Col. 12, L.5-60 wherein the phase is corrected in order for the head to make the head be connected as shown in the Applicant's Specification in paragraph [27].).

Regarding Claim 38, Tuttle et al. teach a method, comprising:

Generating a servo signal with a read head, the servo signal representing servo data and having a phase that represents a connection polarity of the read head (Col. 11, Lines 30-47);

Recovering the servo data from the servo signal (Col. 9, Line 57 to Col. 10, Line 6. Tuttle et al. teach a read channel that reads servo data.);

And determining the phase of the servo signal from the recovered servo data (Col. 11, Lines 30-47. See also Col. 12, L.5-60 wherein the phase is corrected in order for the head to make the head be connected as shown in the Applicant's Specification in paragraph [27].).

Regarding Claim 39, Tuttle et al. teach all the limitations of Claim 38. Tuttle et al. further teach wherein the servo data includes a synchronization mark (Col. 12, Lines 5-8); the determining comprises determining the phase of the servo signal from the recovered synchronization mark (Col. 12, Lines 49-62).

Regarding Claim 40, Tuttle et al. teach all the limitations of Claim 38. Tuttle et al. further teach further comprising generating a signal that indicates the determined phase of the servo signal (Col. 12, Lines 57-62. Tuttle et al. receives the sample and during acquisition, calculates the phase error, therefore a phase must be received in order to calculate a phase error.).

Regarding Claim 41, Tuttle et al. teach all the limitations of Claim 38. Tuttle et al. further teach comprising adjusting the phase of the servo signal to a desired value if the determined phase has an undesired value (Col. 13, Lines 17-24).

Regarding Claim 43, Tuttle et al. teach a method, comprising: calculating a respective path metric for each of no more than two possible states of a binary sequence having pairs and only pairs of consecutive first logic levels and consecutive second logic levels; and determining a surviving path from the calculated path metrics, a recovered binary sequence lying along the surviving path (Col. 13, Lines 1-60, Tuttle et al. teaches the sampling and coding and processing of code pairs 00, 10, 01, 11).

Regarding Claim 44, Cloke et al. teach all the limitations of Claim 43. Cloke et al. further teach wherein the calculating comprises calculating a respective path metric for and only for possible binary states 00 and 11 of the binary sequence (Col. 13, L. 30-38).

Regarding Claims 45 and 47, Cloke et al. teach a method comprising:

Sampling a signal that represents a binary sequence having pairs and only pairs of consecutive logic 0's and logic 1's (Col. 13, Lines 1-60, Tuttle et al. teaches the sampling and coding and processing of code pairs 00, 10, 01, 11);

For each pair of samples, calculating multiple path metrics for no more than two possible states of the binary sequence (Col. 13, Lines 1-60, Tuttle et al. teaches the sampling and coding and processing of code pairs 00, 10, 01, 11);

And determining a surviving path from the calculated path metrics, a recovered binary sequence lying along the surviving path (Col. 13, Lines 1-60, Tuttle et al. teaches the sampling and coding and processing of code pairs 00, 10, 01, 11).

Regarding Claim 46, Cloke et al. teach all the limitations of Claim 46. Cloke et al. further teach wherein the calculating comprises, for each pair of samples: calculating no path metrics for the possible binary states 01 and 10; and calculating multiple two metrics for each of the possible binary states 00 and 11 (Col. 13, Lines 1-60, Tuttle et al. teaches the sampling and coding and processing of code pairs 00, 10, 01, 11).

Regarding Claim 48, Cloke et al. teach all the limitations of Claim 47. Cloke et al. further teach wherein the recovery circuit is operable to recover the binary sequence from the signal by: for each pair of samples, calculating no path metrics for the possible binary states 01 and 10; and for each pair of samples, calculating two respective path metrics for each of the possible binary

states 00 and 11 (Col. 13, Lines 1-60, Tuttle et al. teaches the sampling and coding and processing of code pairs 00, 10, 01, 11)

Regarding Claim 6, Tuttle et al. teach a Viterbi detector, comprising:

An input terminal operable to receive a signal that represents a binary sequence having pairs and only pairs of consecutive first logic levels and consecutive second logic levels (It is inherent that bits are grouped into consecutive group of binary bits.);

And a recovery circuit coupled to the input terminal, the circuit operable to recover the binary sequence from the signal by (Col. 8, Line 67 to Col. 4. Tuttle et al. teach a read channel that recovers binary data.),

Calculating a respective path metric for each of no more than two possible states of the binary sequence and determining a surviving path from the calculated path metrics, the binary sequence lying along the surviving path (Col. 13, Lines 1-60, Tuttle et al. teaches the sampling and coding and processing of code pairs 00, 10, 01, 11. Tuttle et al. teaches determining the path by the use of sampling and further processing of a 2T preamble.).

Regarding Claim 7, Tuttle et al. teach all the limitations of Claim 6. Tuttle et al. further teach comprising:

A register coupled to the recovery circuit (Fig. 7, Elements B166(b) and Col. 10, Lines 46-49 and Col. 11, Lines 51-53);

And wherein the recovery circuit is operable to load the recovered binary sequence into the register (Fig. 7, Elements B166(b) and Col. 10, Lines 46-49 and Col. 11, Lines 51-53).

Regarding Claim 8, Tuttle et al. further teach the first logic level equals logic 1 and the second logic level equals logic 0. (Col. 13, Lines 1-60, Tuttle et al. teaches the sampling and coding and processing of code pairs 00, 10, 01, 11. Tuttle et al. teaches determining the path by the use of sampling and further processing of a 2T preamble.).

Regarding Claim 9, Tuttle et al. further teach wherein the recovery circuit is operable to recover the binary sequence from the signal by calculating a respective path metric for two and only two possible states of the binary sequence (Col. 13, Lines 1-60, Tuttle et al. teaches the sampling and coding and processing of code pairs 00, 10, 01, 11. Tuttle et al. teaches determining the path by the use of sampling and further processing of a 2T preamble.).

Regarding Claim 10, Tuttle et al. further teach wherein the recovery circuit is operable to recover the binary sequence from the signal by calculating a respective path metric for and only for possible binary states 00 and 11 (Col. 13, Lines 1-60, Tuttle et al. teaches the sampling and coding and processing of code pairs 00, 10, 01, 11. Tuttle et al. teaches determining the path by the use of sampling and further processing of a 2T preamble.).

Regarding Claim 11, Tuttle et al. further teach wherein the recovery circuit is operable to recover the binary sequence from the signal according to a PR4 protocol (Col. 13, Lines 1-60, Tuttle et al. teaches the sampling and coding and processing of code pairs 00, 10, 01, 11. Tuttle et al. teaches determining the path by the use of sampling and further processing of a 2T preamble.).

Regarding Claim 12, Tuttle et al. further teach the input terminal is operable to receive samples of the signal; and the recovery circuit is operable to process two samples at a time (Col. 13, Lines 1-60, Tuttle et al. teaches the sampling and coding and processing of code pairs 00, 10,

01, 11. Tuttle et al. teaches determining the path by the use of sampling and further processing of a 2T preamble.).

Regarding Claims 13 and 17, Tuttle et al. teach a Viterbi detector, comprising:

An input terminal operable to receive samples of a signal that represents a binary sequence having pairs and only pairs of consecutive logic 0's and logic 1's (Col. 8, Lines 48-51 and Lines 56-59. Tuttle et al. further teach that the read data is binary data.);

And a recovery circuit coupled to the input terminal and to the register (Fig. 7, Elements B166(b) and Col. 10, Lines 46-49 and Col. 11, Lines 51-53),

Calculating a respective path metric for each of no more than two possible states of the binary sequence and determining a surviving path from the calculated path metrics, the binary sequence lying along the surviving path(Col. 13, Lines 1-60, Tuttle et al. teaches the sampling and coding and processing of code pairs 00, 10, 01, 11. Tuttle et al. teaches determining the path by the use of sampling and further processing of a 2T preamble.).

Regarding Claim 14, Tuttle et al. further teach wherein the recovery circuit is operable to recover the binary sequence from the signal by calculating, for each pair of samples, multiple path metrics for two of the possible binary states and only two of the possible binary states (Col. 13, Lines 1-60, Tuttle et al. teaches the sampling and coding and processing of code pairs 00, 10, 01, 11. Tuttle et al. teaches determining the path by the use of sampling and further processing of a 2T preamble.).

Regarding Claim 15, Tuttle et al. further teach wherein the recovery circuit is operable to recover the binary sequence from the signal by: for each pair of samples, calculating multiple path metrics for the possible binary states 00 and 11 and only the possible binary states 00 and 11

(Col. 13, Lines 1-60, Tuttle et al. teaches the sampling and coding and processing of code pairs 00, 10, 01, 11. Tuttle et al. teaches determining the path by the use of sampling and further processing of a 2T preamble.).

Regarding Claim 16, Tuttle et al. further teach wherein the recovery circuit is operable to recover the binary sequence from the signal by: for each pair of samples, calculating no path metrics for the possible binary states 01 and 10; and for each pair of samples, calculating two respective path metrics for each of the possible binary states 00 and 11 (Col. 13, Lines 1-60, Tuttle et al. teaches the sampling and coding and processing of code pairs 00, 10, 01, 11. Tuttle et al. teaches determining the path by the use of sampling and further processing of a 2T preamble.).

Regarding Claim 18, Tuttle et al. further teach wherein the recovery circuit is operable to recover the binary sequence from the signal by calculating, for each pair of samples, the difference and only the difference between the path metrics for the two possible states (Col. 13, Lines 1-60, Tuttle et al. teaches the sampling and coding and processing of code pairs 00, 10, 01, 11. Tuttle et al. teaches determining the path by the use of sampling and further processing of a 2T preamble.).

Regarding Claim 19, Tuttle et al. teach all the limitations of Claim 17. Tuttle et al. further teach wherein the recovery circuit is operable to recover the binary sequence from the signal by calculation, for each pair of samples, of the difference between the path metrics for the two possible states 00 and 11 (Col. 13, Lines 1-60, Tuttle et al. teaches the sampling and coding and processing of code pairs 00, 10, 01, 11. Tuttle et al. teaches determining the path by the use of sampling and further processing of a 2T preamble.).

Regarding Claim 20, Tuttle et al.. teach all the limitations of Claim 17. Tuttle et al. further teach wherein the recovery circuit is operable to recover the binary sequence from the signal by: for each pair of samples, calculating no path metrics for or difference metric between possible binary states 01 and 10; and for each pair of samples, calculating the difference between the path metrics for possible binary states 00 and 11 (Col. 13, Lines 1-60, Tuttle et al. teaches the sampling and coding and processing of code pairs 00, 10, 01, 11. Tuttle et al. teaches determining the path by the use of sampling and further processing of a 2T preamble.).

Regarding Claims 24 and 35, Tuttle et al. teach all the limitations of Claim 21 and 33, respectively. Tuttle et al. further teach:

> The synchronization mark has pairs and only pairs of consecutive logic 0's and logic 1's (Col. 8, Lines 48-51 and Lines 56-59. Tuttle et al. further teach that the read data is binary data.);
>
> And the Viterbi detector comprises,
>
> A recovery circuit operable to recover the synchronization mark from the samples of the servo signal by (Col. 4, Lines 54-67 and Col.. 7, Lines 33-38and Col. 9, Lines 50-59. Reed et al. teach a circuit that receives inputted data from the head and detects the polarity of the servo signal from that data.),
>
> Calculating a respective path metric for each of no more than two possible states of the binary sequence and determining a surviving path from the calculated path metrics, the binary sequence lying along the surviving path (Col. 13, Lines 1-60, Tuttle et al. teaches the sampling and coding and processing of code pairs 00, 10, 01, 11. Tuttle et al. teaches determining the path by the use of sampling and further processing of a 2T preamble.).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 25, 26 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tuttle et al. (US Patent No. 6, 108, 151) in view of Cloke et al. (US Patent No. 5, 822, 143).

Regarding Claims 25, 26 and 42, Tuttle et al. and Cloke et al. teach all the limitations of Claim 21 and 38, respectively. Tuttle et al. fail to teach wherein the servo data includes a synchronization mark; and the determining comprises, comparing the recovered synchronization mark to an ideal synchronization mark on a bit-by-bit basis, determining that the servo signal is in phase if the number of mismatching bits is less than or equal to a first predetermined threshold, and determining that the servo signal is out of phase if the number of mismatching bits is greater than or equal to a second predetermined threshold. However, this feature is well known in the art as disclosed by Cloke et al., wherein it teaches wherein the servo data includes a synchronization mark; and the determining comprises, comparing the recovered synchronization mark to an ideal synchronization mark on a bit-by-bit basis, determining that the servo signal is in phase if the number of mismatching bits is less than or equal to a first predetermined threshold, and determining that the servo signal is out of phase if the number of mismatching bits is greater than or equal to a second predetermined threshold (Pat. No. 5, 822, 143; See Fig. 1A and Col. 1, Lines 45-48, Lines 53-59 and Col. 1, Line 60 to Col. 2, Line 19). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify

Tuttle et al.'s invention to use a path metric in order to effectively estimate the most likely sequence of symbols.

4. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tuttle et al. (US Patent No. 6, 108, 151) in view of Reed et al. (US Patent No. 6, 490, 110). Tuttle et al. teach all the limitations of Claim 33. Tuttle et al. fail to teach wherein: the comparator is coupled to the sampling circuit; and if the determined phase is opposite to a desired phase, then the sampling circuit is operable to invert the samples of the servo signal. However, this feature is well known in the art as disclosed by Reed et al., wherein it teaches a circuit that changes the polarity of the signal (Pat. No. 6, 490, 110; Col. 5, Lines 3-11). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Tuttle et al.'s invention in order to correct the polarity for effective detection of polarity.

Response to Arguments

Applicant's arguments with respect to claims 1-50 have been considered but are not moot. However, the rejections to Claims 6-20 and 24 and 34 and 35 are now in view of Tuttle et al.

Applicant argues that the invention does have a first Viterbi detector (100) and a second Viterbi detector. However, the Specification is not clear about where the mentioned "first Viterbi" and "second Viterbi" are in the Specification. Examiner suggests to the Applicant to specify in the specification the phrases "first Viterbi" and "second Viterbi" as Claimed in the Claims in order to avoid confusion in the Claim language.

Applicant also argues that in Claims 1, 49 "Reed neither discloses nor suggests a determination operable to determine connection polarity of a read-write head from the recovered servo data". Examiner cannot concur because Reed doeas teach a head connected to a servo

circuit in which the polarity and head connection is found according the definition to head connection that is found in the Specification in paragraph [27] (See Col. 4, Lines 54-67 and Col. 11, Lines 54-67. Reed et al. teach of a circuit that determines if the polarity pulses are positive or negative. And Col. 13, L. 11-58, wherein the phase is corrected in order for the head to make the head be connected as shown in the Applicant's Specification).

Regarding Claims 21, 27 and 38, Applicant exposes the same argument as in Claims 1 and 49. Examiner cannot concur because of the same reasons as exposed in Claim 1 and 49 (See Col. 20, Lines 15-22. Tuttle et al. teach that the Viterbi detector could also be used for synchronously detecting data. See also Col. 12, L.5-60 wherein the phase is corrected in order for the head to make the head be connected as shown in the Applicant's Specification in paragraph [27].).

Regarding Claims 6-20, 24, 34 and 35 arguments have been considered moot. However, these Claims are now rejected under Tuttle et al. (US Patent No. 6, 108, 151).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenda P. Rodriguez whose telephone number is (703) 305-8411. The examiner can normally be reached on Monday thru Thursday: 7:00-5:00; alternate Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Hudspeth can be reached on (703) 308-4825. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

gpr
01/25/2005.

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